In the Claims

    This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Currently Amended) A method of performing a dot product
2 operation with rounding and shifting in a microprocessor in
3 response to a single rounding dot product instruction, the method
4 comprising the steps of:
5   fetching a first pair of elements and a second pair of
6 elements;
7   forming a first product of the first pair of elements and a
8 second product of the second pair of elements;
9   ~~combining the first product with the second product to form a~~
10 ~~combined product;~~
11   <u>combining the first product with the second product to form a</u>
12 <u>combined product and</u> rounding the combined product to form an
13 intermediate result <u>via an arithmetic circuit having a first input</u>
14 <u>receiving said first product, a second input receiving said second</u>
15 <u>product and a carry input to a mid-position receiving said rounding</u>
16 <u>value to form the intermediate result;</u> and
17   <u>right</u> shifting the intermediate result a selected amount to
18 form a final result.

    Claims 2 and 3.   (Canceled)

1   4.   (Currently Amended) The method of Claim ~~3~~ <u>1</u>, wherein the
2 rounding value is 2^n and the selected shift amount is n+1.

1   5.   (Original) The method of Claim 4, wherein n has a fixed
2 value of fifteen.

    Claims 6 to 8. (Canceled)

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1   9. (Currently Amended) The method of Claim 1, wherein the

2 ~~step~~ steps of forming the first product and forming the second

3 product treats a one of the first pair of elements as a signed

4 number value and treats another one of the first pair of elements

5 as an unsigned number value.

1   10. (Original) The method of Claim 1, wherein the step of

2 combining comprises subtracting the product of second pair of

3 elements from the product of first pair of elements.

1   11. (Original) The method of Claim 1, wherein the step of

2 combining comprises adding the product of second pair of elements

3 to the product of first pair of elements.

   12. (Canceled)

1   13. (Currently Amended) A digital system having a

2 microprocessor operable to execute a rounding dot product

3 instruction, wherein the microprocessor comprises:

4   storage circuitry for holding pairs of elements;

5   a multiply circuit connected to receive a first number of

6 pairs of elements from the storage circuitry in a first execution

7 phase of the microprocessor responsive to the dot product

8 instruction, the multiply circuit comprising a plurality of

9 multipliers equal to the first number of pairs of elements;

10   an arithmetic circuit having a plurality of inputs each

11 connected to receive a corresponding one of the plurality of

12 products from the plurality of multipliers~~, the arithmetic circuit~~

13 ~~having a provision~~ and a mid-position carry input for mid-position

14 rounding responsive to the rounding dot product instruction; and

<center>— 3 —</center>

15   a shifter connected to receive an output of the arithmetic
16   circuit, the shifter operable to shift a selected amount in
17   response to the rounding dot product instructions.

     Claims 14 and 15.   (Canceled)

1   16.   (Currently Amended) The method of Claim 3 1, wherein:
2   the step of shifting further includes sign extends extending
3   the intermediate result.

1   17.   (New) The digital system of Claim 13, wherein:
2   the shifter right shifts the output of the arithmetic circuit
3   by the selected amount and sign extends the output of the
4   arithmetic circuit.

1   18.   (New) A method of performing a dot product operation with
2   rounding and shifting in a microprocessor in response to a single
3   rounding dot product instruction, the method comprising the steps
4   of:
5   fetching a first pair of elements and a second pair of
6   elements;
7   forming a first product of the first pair of elements treating
8   a one of the first pair of elements as a signed number value and
9   treating another one of the first pair of elements as an unsigned
10   number value;
11   forming a second product of the second pair of elements
12   treating a one of the first pair of elements as a signed number
13   value and treating another one of the first pair of elements as an
14   unsigned number value;
15   combining the first product with the second product to form a
16   combined product;

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17   rounding the combined product to form an intermediate result;
18   and
19   shifting the intermediate result a selected amount to form a
20   final result.

1   19.   (New) The method of Claim 18, wherein the step of
2   rounding adds a rounding value to the combined product via an
3   arithmetic circuit having a first input receiving said first
4   product, a second input receiving said second product and a carry
5   input to a mid-position receiving said rounding value to form the
6   intermediate result, and wherein the step of shifting shifts the
7   intermediate result right by a selected shift amount.

1   20.   (New) The method of Claim 19, wherein the rounding value
2   is 2^n and the selected shift amount is n+1.

1   21.   (New) The method of Claim 20, wherein n has a fixed value
2   of fifteen.

1   22.   (New) The method of Claim 19, wherein:
2   the step of shifting further includes sign extending the
3   intermediate result.

1   23.   (New) The method of Claim 18, wherein the step of
2   combining comprises subtracting the product of second pair of
3   elements from the product of first pair of elements.

1   24.   (New) The method of Claim 18, wherein the step of
2   combining comprises adding the product of second pair of elements
3   to the product of first pair of elements.

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